An Efficient Full Digital Frequency Hopping Demodulator Based on Polyphase Filter Banks

fredric harris, Xiaofei Chen, Elettra Venosa
San Diego State University
fred.harris@sdsu.edu, chenxiaofei_sdsu@yahoo.com, elettra.venosa@unina2.it

ABSTRACT

Frequency-hopped spread spectrum (FHSS) is a method of transmitting radio signals by rapidly switching a carrier among many frequency channels, using a pseudorandom sequence known to both transmitter and receiver. FHSS systems present a number of advantages which include resistance to narrow band interference, being difficult to intercept and being capable of sharing spectrum with many types of existing transmissions. Today, FHSS technique is widely used in many military radio applications as well as commercial applications in the license-free industrial, scientific and medical bands. In this paper, we propose a full digital FHSS demodulator, which allows us to de-hop the hopping sequence in the digital domain while keeping the system operating at lower sampling rates. By designing the receiver in the digital domain, the proposed architecture enables a number of advantages over the legacy FHSS radios.

Index Terms: *frequency hopped spread spectrum, polyphase channelizer, parallel PN search*

1. INTRODUCTION

Frequency-hopped spread spectrum (FHSS) transmits radio signals by switching its carrier frequency among many possible frequencies that are determined by a pseudorandom sequence known to both transmitter and receiver. Because of its excellent anti-jamming and anti-interception capabilities [1], [2], FHSS communication systems are commonly found in many military radio applications. Meanwhile, it is also being widely used in a number of today's civilian applications, i.e. Bluetooth piconet (IEEE 802.15.1) [3], and wireless local area network (IEEE 802.11) [4].

Over the past 30 years, a considerable amount of research has appeared in the literature in dealing with this topic over a wide range of disciplines, i.e. system performances under various configurations (channel conditions, jammer setups, etc.), hopping sequence design [5] [6], etc, and spectrum sharing /multiplexing [7], [8], etc. However, there is only limited amount of early research dealing with the physical layer design of FHSS radios, especially from the synchronization aspects. Moreover, a great majority of the following studies and research results were based on the earlier developed physical layer and most of the results were obtained by assuming perfect synchronization. The most widely known FHSS radio prototypes as well as their corresponding synchronization schemes can be found in [9], [10]. A high level block diagram is shown in Figure 1. It can be seen from Figure 1 that the frequency shift keying (FSK) is often used as the underlying modulation scheme. The M-*ary* signaling is then shifted pseudo-randomly by the frequency synthesizer over some frequency hopping band. This system is called MFSK/FH system. The demodulation of a MFSK/FH signal can be partitioned into two steps. The first step is to de-hop the pseudorandom hopping sequence. The second step is to demodulate the underlying FSK signal. The conventional frequency hopping modem implements the first step by using analog mixers to down-convert the modulated FSK signal to the intermediate frequency or baseband, and then uses an analog or a digital FSK demodulator to extract the received information. The reason for using analog mixers in the first step is to avoid processing signals at very high sample rate that would be required to satisfy the Nyquist criteria for the spectral span of hopping frequencies. As a consequence, the conventional FHSS receivers suffer from analog artifacts which affect the system performance as well as limit flexibility to implement innovative signal options.

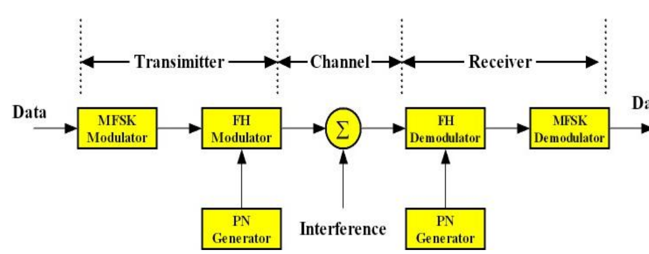

Figure 1. High level view of MFSK/FH system

In this paper, we describe a full digital FHSS demodulator, which allows us to de-hop the FHSS signal in the digital domain while keeping the system operating at lower sampling rates. The remainder of the paper is organized as follows. In Section 2, an *M*-path channelizer based demodulator structure will be proposed. In Section 3, the benefits brought by the new system will be discussed. The simulation results will be shown in Section 4 and the conclusion will be given in Section 5.

2. PROPOSED DEMODULATOR STRUCTURE

As mentioned earlier, the demodulation of a MFSK/FH signal requires two steps: de-hopping and MFSK demodulation. Conventionally, the de-hopping is performed in the analog domain. It consists of an analog mixer, whose center frequency varies according to the hopping pattern determined by the PN sequence; and a low-pass analog band limiting filter, whose bandwidth is matched to the MFSK signal bandwidth [9]. Notice that the de-hopping process is a collection of down converting and filtering processes, which can be easily achieved by an *M*-path down converting channelizer. Furthermore, the task of demodulating an MFSK signal is to determine the frequency deviations, which is commonly achieved by implementing a bank of band-pass filters and envelop detectors [9]. In this section, we first review the concept of the multirate polyphase down converting channelizer; then we show the proposed demodulator structure based on multirate channelizer.

2.1 *M*-Path Down Converting Channelizer

A polyphase down sampling channelizer simultaneously down converts and down samples *M* equally spaced, fixed bandwidth signals [11]. Figure 2 shows its complete structure formed by an *M*-port commutator, an *M*-path partitioned low-pass prototype filter and an *M*-point inverse discrete Fourier transform (IDFT) block. For computational efficiency the IDFT is implemented with the IFFT algorithm.

In this engine, the commutator delivers *M* consecutive samples to the *M* input ports of the *M*-path filter performing the signal sample rate reduction which causes *M* spectral folds in the frequency domain. With an output sample rate of f_S/M, all *M* multiples of the output sample rate alias to base band (DC). The alias terms in each arm of the *M*-path filter exhibit unique phase profiles due to their distinct center frequencies and the time offsets of the different down sampled time series delivered to each commutator port. In particular, each of the aliased term exhibits a phase shift equal to the product of its center frequency *k* with its path time delay *r*. These phase shifts are shown in Eq. (1), where f_S is the sample rate at the input to the polyphase down converter. The partitioned *M*-path filter aligns the time

$$\varphi(r,k) = -\omega_k \Delta T_r = -2\pi \frac{f_S}{M} k r T_s = -\frac{2\pi}{M} r k \qquad (1)$$

origin of the sampled data sequences delivered by the input commutator to a single common output time origin. This task is accomplished by the all-pass characteristics of the *M*-path partitioned filter that applies the required differential time delay to the individual input time series. Finally the IFFT block performs the equivalent of a beam-forming operation: the coherent summation of the time aligned signals with at each output port with selected phase profile. The phase coherent summation of the outputs of the *M*-path filters separates the various aliases residing in each path by constructively summing the selected aliased frequency components located in each path, while simultaneously destructively canceling the remaining aliased spectral components. The IFFT block extracts, in each arm, from the myriad of aliased signals only the alias with the particular matching phase profile. Summarizing, we can describe the three basic operations performed by a standard polyphase down converter as: sample rate change, due to the input commutator; bandwidth reduction, due to the *M*-path partitioned filter weights and Nyquist zone selection, due to the IFFT block.

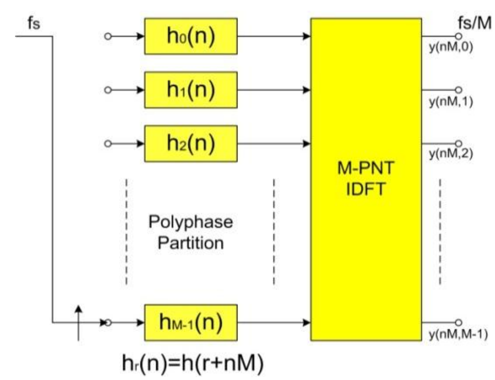

Figure 2. Standard *M*-path Polyphase Down Converting Channelizer

2.2 Proposed MFSK/FH Demodulator

Having realized that the *M*-path polyphase down converting channelizer is an efficient structure for implementing *M* band-pass filters together with *M* down converters, in this section we will show this structure is an excellent or perhaps one of the best candidates for implementing FH demodulator digitally.

We know that the MFSK symbol is modulated onto different carrier frequencies scheduled by the PN sequence. Conventionally, the first step of demodulating an MFSK/FH signal is to de-hop the received signal by means of using an analog mixer whose frequency is changed according to the locally generated PN sequence as shown in Figure 3. In general, there are two reasons for which the structure shown in Figure 3 was chosen as the “standard” FH demodulator over other possibilities during the analog days. Since the total number of possible hopping frequencies can be very large, it is extremely expensive to build matched filters for all possible hopping frequencies in the analog domain [9]. The second reason is the direct conversion of analog design into digital design does not necessarily favor us in terms of cost, since one might need to process considerable amount of samples, which is quite difficult even using today’s technology.

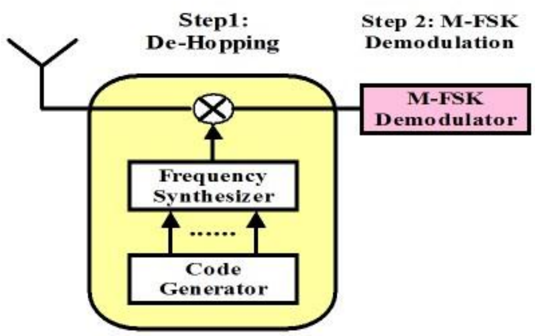

Figure 3. Conventional FH demodulator

However, the M-path channelizer allows us to de-hop the hopping sequence in the digital domain while keeping the system operating at lower sampling rates. The idea is to design an M-path polyphase down-converting channelizer with each channel centered on the designed hopping center frequencies as shown in Figure 4. The M-path channelizer aliases or de-hops all hopping center frequencies to baseband while simultaneously performing M-to-*1* down sampling from the input sample rate. Thus the system can be operated at same low output sample rate as the conventional approach does. Similarly to the de-hopping process, the M-path channelizer happens to be the matched filter for MFSK signal also. Thus, we can take advantage of this efficient structure twice in our demodulator.

Shown in Figure 5 is our proposed FHSS demodulator. We placed an M-path channelizer to channelize M possible hopping frequencies. Following this front end M-path channelizer is the PN sequence synchronization block, which is a commutator that is also responsible for acquiring and tracking the PN sequence. When the locally generated PN sequence is synchronized with the received MFSK/FH signal, this commutator essentially delivers the de-hopped FSK signal to the next stage channelizer. Assuming there are P possible tones or frequency deviations for the FSK signal, a P-path channelizer is adopted with each channel center matched to P possible FSK tones. The following decision process is similar to the conventional approach, i.e. integration and selection.

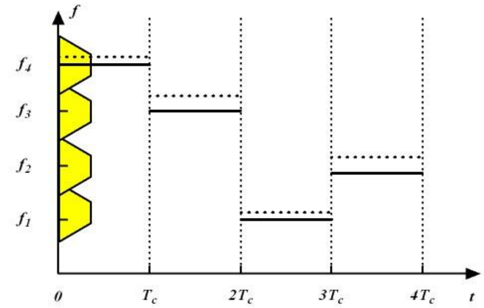

Figure 4. M-path Channelizer Aliases Hopping Frequencies onto Baseband

3. BEFINITES ENABLED BY THE PROPOSED STRUCTURE

In the previous section, a full digital FHSS demodulator structure has been presented. Now, we discuss the advantages this structure offers. Whenever we upgrade the physical layer design, some surprising added features appear. Here, we ignore the analog defects from the legacy design and focus our scope on synchronization and system level performance.

3.1 Fast Acquisition Based on Parallel Search

In order to establish the link between the transmitter and the receiver, both ends should acquire and lock to the same PN sequence, so that the received signal can be correctly de-hopped. At the receiver end, the radio has to have an acquisition scheme to acquire the PN sequence; it must also be equipped with a PN tracking loop [9] [12], to remain in lock with the PN sequence. The current physical layer acquisition scheme is based on serial search scheme [9], [10], which is a direct result of legacy FH demodulator shown in Figure 3. During the acquisition process, the receiver tunes the phase of the PN code generator in order to be aligned with the incoming FH signal. It has been shown in [13] that the expected acquisition time based on serial search is :

$$\overline{T_{acq}} = \frac{(2-P_D)(1+KP_{FA})}{P_D}(N_C\lambda T_C) \quad (2)$$

where λ is the number of chips examined during each correlations, T_c is the chip duration, P_D is probability of correct detection, P_{FA} is probability of false alarm, N_c is the number of chips contained in the uncertainty region to be searched over. $K\lambda T_c$, where K >>1 is the time needed to verify a detection,i.e, in the event of a false alarm .$K\lambda T_c$ is the time penalty [9].

The parallel search scheme proposed in [14] had always been viewed as a conceptual model because it was too

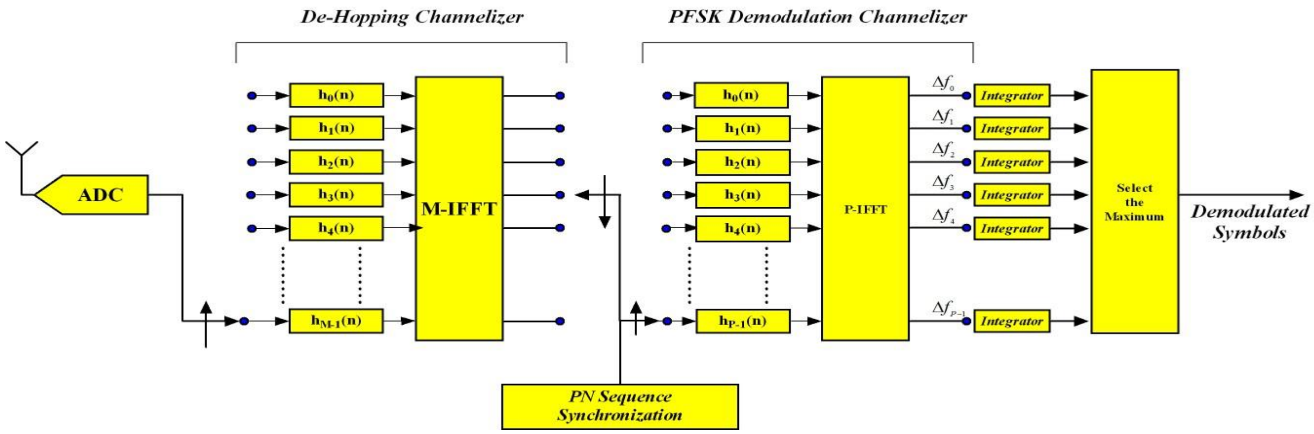

Figure 5. Proposed full digital FHSS demodulator

expensive and unrealistic to build so many band-pass filters in the analog domain in order to accommodate all possible hopping frequencies [9], [10]. However, when using *M*-path channelizer as FH demodulator, we can easily implement *M* band-pass filters together with *M* down converters and have access to all hopping channels simultaneously. In other words, the *M*-path channelizer front end enables the parallel search acquisition mode, whose expected acquisition time, shown in Eq. (3), is significantly shorter than serial search scheme, where λ is the number of chips examined during

$$\overline{T_{acq}} = \frac{\lambda T_C}{P_D} \tag{3}$$

each correlations, T_c is the chip duration, and P_D is probability of correct detection.

3.2 Diversity Hopping

By implementing the de-hopping circuit with *M*-path polyphase channelizer, we have access to each of the *M* hopping band simultaneously. Thus, the receiver automatically supports and benefits from two diversity modes, namely multiple simultaneous hopping sequences and diversity hopping. In the multiple simultaneous hopping mode, the receiver can receive FHSS signals from more than one transmitter that are using different sets of hopping sequences. In the diversity hopping mode, the same data can be modulated onto different sets of hopping sequences, while the receiver can de-hop all sets of hopping sequences and take advantage of the frequency diversity to increase the robustness and the overall performance of the system.

4. SIMULATION RESULTS

In this section we present the simulation results based on the proposed MFSK/FH demodulator. Assuming the incoming MFSK/FH signal has 16 possible hopping frequencies and the tone spacing between adjacent hopping tones is 0.8 *MHz*. And, we use 8-FSK as the underlying modulation scheme whose tone spacing is set to be 80 *kHz*.

The generated incoming signal is shown in Figure 6. Subplot 1 of Figure 6 shows the frequency hopping profile over each symbol; subplot 2 and 3 of Figure 6 show the time series and the spectrum of the generated frequency hopping signal. The received signal is sampled at 16 *MHz*, and we use a 20-channel polyphase channelizer as FH demodulator. Figure 7 shows all the time series observed at each output port of the de-hopping channelizer. We can see all FSK symbols occur on different time, which implies the signal has been de-hopped. Figure 8 zooms into the de-hopping channelizer output port corresponding to 1.2 *MHz* hopping channel. We can see the received 8-FSK signal and its envelope in detail. We then feed this 1.2*MHz* signal shown in Figure 8 into the FSK demodulation channelizer. Figure 9 shows the non-empty channel outputs from the FSK demodulation channelizer. We ascertained that the three symbols seen from the 1.2 *MHz* de-hopping output from Figure 8 to have frequency deviations at -200 *kHz*, -40 *kHz*, and 120 *kHz*.

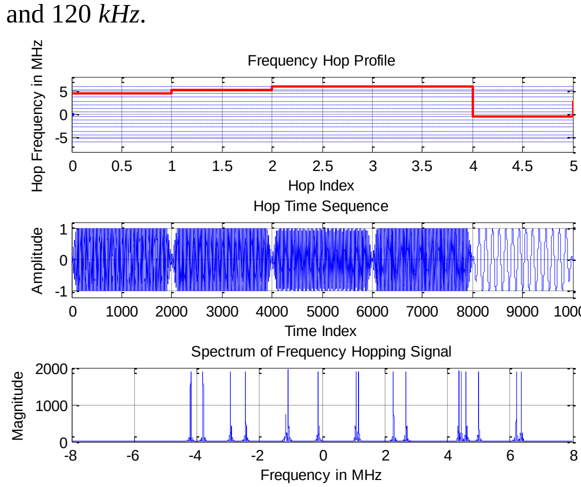

Figure 6. Frequency Hopping Profile and Hop Time Series

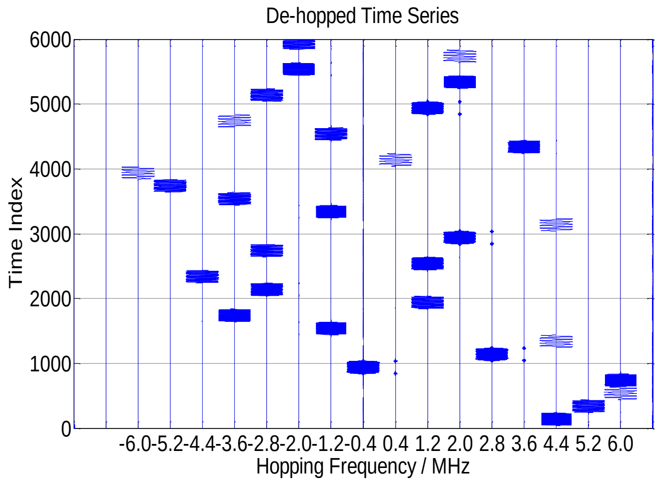

Figure 7. De-hopped Signal Time Series Plotted at All Output Ports of De-hopping Channelizer

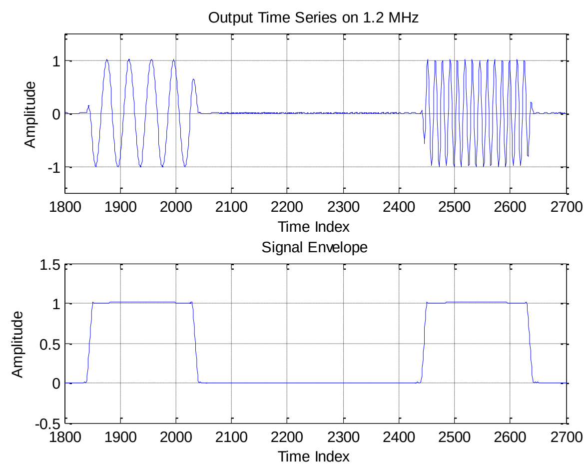

Figure 8. Zoom into 1.2 *MHz* Hopping Center

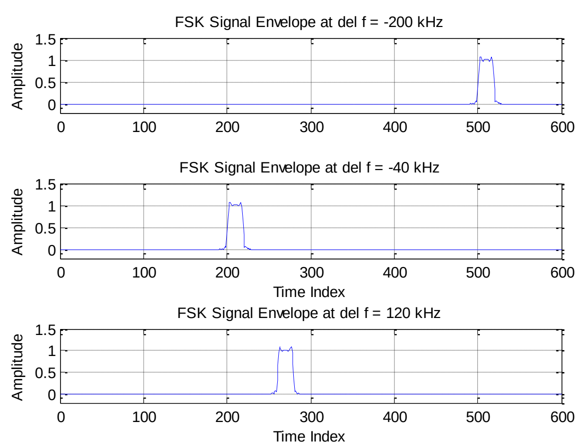

Figure 9. 8-FSK Demodulation Channelizer Output for 1.2 *MHz* Hopping Center

5. CONCLUSION

In this paper we presented a full digital FHSS demodulator based on *M*-path polyphase channelizer. The proposed structure not only efficiently demodulates the frequency hopped signals but also enables fast acquisition and provides added features that could not be achieved by conventional FHSS radio. The simulation results also show the proper functioning of the proposed demodulator structure.

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